

In the Claims

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Cancel claims 1-56.

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New Claims

Aa

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57. An integrated circuit comprising hemispherical grain platinum.

58. An integrated circuit comprising:

a monocrystalline silicon substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer being continuous over an area of the substrate that comprises at least about 4×10^6 square Angstroms and comprising pedestals that are at least about 300\AA tall within the area.

59. The circuit of claim 58 wherein the platinum layer comprises hemispherical grain platinum.

60. The circuit of claim 58 wherein the area of the substrate comprises a square.

61. An integrated circuit comprising:

a monocrystalline silicon substrate; and

a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

A2
cont.

1 62. The circuit of claim 61 wherein the platinum layer has a
2 thickness of at least about 600Å.

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4 63. The circuit of claim 61 wherein the platinum layer has a
5 thickness of greater than or equal to about 400Å.

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7 64. The circuit of claim 61 wherein the platinum layer has a
8 thickness of greater than or equal to about 100Å.

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10 65. The circuit of claim 61 further comprising an adhesion layer
11 between the platinum layer and the substrate, the adhesion layer
12 comprising at least one of titanium nitride, iridium, rhodium, ruthenium,
13 platinum, palladium, osmium, silver, rhodium/platinum alloy, IrO₂, RuO₂,
14 RhO₂, or OsO₂.

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16 66. The circuit of claim 61 wherein the pedestals terminate in
17 dome-shaped tops.

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19 67. The circuit of claim 61 wherein the pedestals terminate in
20 hemispherical tops.

Aa
cont.

1 68. A capacitor comprising:
2 a first capacitor electrode over a monocrystalline silicon substrate;
3 a second capacitor electrode;
4 a dielectric layer between the first and second capacitor electrodes;
5 and

6 wherein at least one of the first and second capacitor electrodes
7 comprises a roughened platinum layer, the roughened platinum layer
8 having a thickness of from about 400Å to about 1000Å and comprising
9 pedestals that are at least about 300Å tall.

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11 69. The capacitor of claim 68 wherein the roughened platinum
12 layer comprises hemispherical grain platinum.

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14 70. The capacitor of claim 68 wherein the roughened platinum
15 layer is over a surface and is continuous over an area of the surface
16 that is at least about 4×10^6 square Angstroms.

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18 71. The capacitor of claim 70 wherein the area comprises a
19 square.

A2
cont.

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72. A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes;

and

wherein at least one of the first and second capacitor electrodes comprises a roughened platinum layer, the roughened platinum layer having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the platinum layer.

73. The capacitor of claim 72 wherein both capacitor electrodes comprise platinum, but only one of the capacitor electrodes comprises the roughened platinum layer.

74. The capacitor of claim 72 wherein both capacitor electrodes comprise roughened platinum layers.

75. The circuit of claim 72 wherein the pedestals terminate in dome-shaped tops.

A2
conc.

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76. The circuit of claim 72 wherein the pedestals terminate in

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hemispherical tops.

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